UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,113	07/12/2000	Pai-Hung Pan	2915.3US (96-0149.2)	1710

7590 10/23/2002

Joseph A Walkowski
Trask Britt
P O Box 2550
Salt Lake City, UT 84110

EXAMINER
BROWN, CHARLOTTE A

ART UNIT	PAPER NUMBER
1765	14

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

AC 14

Office Action Summary	Application No. 09/614,113	Applicant(s) Pan et al.
	Examiner Charlotte Brown	Art Unit 1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 17, 2002*.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *3-22* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *3-22* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 12
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Applicant's arguments with respect to claims 3-22 have been considered but are moot in view of the new ground(s) of rejection.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Segawa et al. (US 5,428,244) in view of Chang (US 5,438,006) and further in view of Possin et al. (US 4,704,783).

Segawa discloses a method of manufacturing a semiconductor device having a silicon rich dielectric layer. A silicon substrate is provided. A gate silicon dielectric layer composed of SiO_2 is grown over the silicon substrate. A polysilicon layer is formed on the surface of the gate dielectric layer. Ions of gate impurities are implanted into the polysilicon layer. A tungsten silicide layer is deposited on the surface on the polysilicon layer . This reads on the applicant's limitation of depositing a metallic silicide film in non-annealed state atop the polysilicon layer. A silicon oxide layer, a dielectric cap layer, is formed on the surface of the polysilicon layer by means of a CVD process (Column 7, lines 7-24). The silicon oxide film is deposited at a temperature of 840^0C. Patterns are formed upon the dielectric cap layer. Upon the completion of

the transferring of patterns, the polysilicon layer, the tungsten silicide film, and the silicon oxide layer are etched sequentially (Column 7, lines 49-52). In one example of the invention, the tungsten silicide layer and the silicon oxide layer are formed from SH_2CL_2 gas. The tungsten silicide layer is formed at a temperature from 500^0C to 600^0C. The SH_2CL_2 gas is introduced in the chamber not only at the step of forming the tungsten silicide but also at the step of forming the silicon oxide layer (Column 13, lines 51-53). Since both the silicon oxide layer and tungsten silicide layer are formed from the SH_2CL_2 gas, the two layers have the same deposition temperature (Column 14, lines 5-8). This reads on the applicant's limitation of forming the cap dielectric layer over the metallic silicide film at a temperature below about 600^0C.

Unlike the claimed invention, Segawa does not teach a method of stripping a resist layer.

Chang teaches a method for fabrication a reduced-height gate stack. A gate oxide layer and a surrounding field oxide layer is formed over a semiconductor substrate. The field oxide layer provides isolation between adjacent transistors. A layer of doped silicon is formed over the oxide layers. A refractory metal layer such as tungsten silicide is formed over the polysilicon layer. A silicon dioxide layer is formed over the metal layer. A layer of photoresist is formed over the oxide layer. The photoresist layer is patterned to form photoresist masks. The photoresist masks are removed in a conventional manner (Column 2, lines 24-45). This reads on the applicant's limitation of stripping the photoresist layer.

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Segawa by using the method of stripping the resist as taught by

Chang. The additional step of stripping the resist would have been expected in order to form a gate stack over the semiconductor substrate.

Unlike the claimed invention, neither Segawa nor Chang teach a method of depositing a dielectric cap layer at a temperature below about 600^{0}C.

Possin teaches a method for fabricating a field effect transistor. A passivating cap layer is provided over a substrate. The cap comprises silicon nitride which is deposited by plasma chemical vapor deposition at a temperature of approximately 150^{0}C (Column 4, lines 1-17).

It is the Examiner's position that a person having ordinary skill in the art would have found it obvious to modify Segawa and Chang with the method of depositing a dielectric cap layer below 600^{0}C as taught by Possin in order to effectively deposit the silicon nitride layer by plasma chemical vapor deposition (Column 4, lines 10-13).

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (US 6,087,254 and US 6,137,130)

5. Any inquiry concerning this communication from the Examiner should be directed to Charlotte A. Brown whose telephone number is 703-305-0727. The Examiner can normally be reached during the hours of 9:00AM to 6:30PM.

The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9310 for regular communications and 703-872-9311 for After Final communications.

CAB

October 21, 2002

BENJAMIN L. UTECH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700